# 3.3 V 1:2 AnyLevel<sup>™</sup> Input to LVDS Fanout Buffer / Translator

### Description

The NB6N11S is a differential 1:2 Clock or Data Receiver and will accept AnyLevel input signals: LVPECL, CML, LVCMOS, LVTTL, or LVDS. These signals will be translated to LVDS and two identical copies of Clock or Data will be distributed, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB6N11S is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications.

The NB6N11S has a wide input common mode range from GND + 50 mV to V<sub>CC</sub> – 50 mV. Combined with the 50  $\Omega$  internal termination resistors at the inputs, the NB6N11S is ideal for translating a variety of differential or single–ended Clock or Data signals to 350 mV typical LVDS output levels.

The NB6N11S is functionally equivalent to the EP11, LVEP11, SG11 or 7L11M devices and is offered in a small, 3 mm X 3 mm, 16–QFN package. Application notes, models, and support documentation are available at <u>www.onsemi.com</u>.

The NB6N11S is a member of the ECLinPS MAX<sup>TM</sup> family of high performance products.

### Features

- Maximum Input Clock Frequency > 2.0 GHz
- Maximum Input Data Rate > 2.5 Gb/s
- 1 ps Maximum of RMS Clock Jitter
- Typically 10 ps of Data Dependent Jitter
- 380 ps Typical Propagation Delay
- 120 ps Typical Rise and Fall Times
- Functionally Compatible with Existing 3.3 V LVEL, LVEP, EP, and SG Devices
- These are Pb-Free Devices

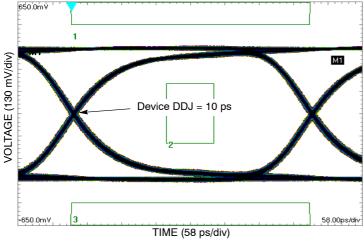
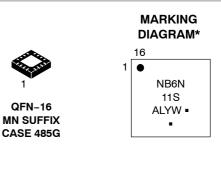


Figure 2. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23-1}$  (V<sub>INPP</sub> = 400 mV; Input Signal DDJ = 14 ps)



# **ON Semiconductor®**

http://onsemi.com



A = Assembly Location

- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb–Free Package

(Note: Microdot may be in either location) \*For additional marking information, refer to Application Note AND8002/D.

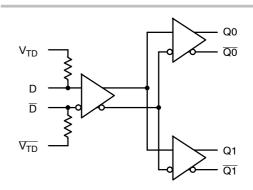


Figure 1. Logic Diagram

# **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

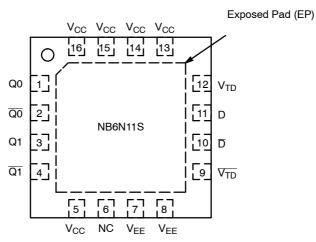


Figure 3. NB6N11S Pinout, 16-pin QFN (Top View)

#### Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	Q0	LVDS Output	Non-inverted D output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
2	<u>Q0</u>	LVDS Output	Inverted D output. Typically loaded with 10 $\Omega$ receiver termination resistor across differential pair.
3	Q1	LVDS Output	Non–inverted D output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
4	<u>Q1</u>	LVDS Output	Inverted D output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
5	V <sub>CC</sub>	-	Positive Supply Voltage
6	NC		No Connect
7	V <sub>EE</sub>		Negative Supply Voltage
8	V <sub>EE</sub>		Negative Supply Voltage
9	$\overline{V_{TD}}$	-	Internal 50 $\Omega$ termination pin for $\overline{D}$
10	D	LVPECL, CML, LVDS, LVCMOS, LVTTL	Inverted Differential Clock/Data Input (Note 1)
11	D	LVPECL, CML, LVDS, LVCMOS, LVTTL	Non-inverted Differential Clock/Data Input (Note 1)
12	V <sub>TD</sub>	_	Internal 50 $\Omega$ termination pin for $\overline{D}$
13	V <sub>CC</sub>	_	Positive Supply Voltage
14	V <sub>CC</sub>	-	Positive Supply Voltage
15	V <sub>CC</sub>	-	Positive Supply Voltage
16	V <sub>CC</sub>	-	Positive Supply Voltage
EP			Exposed pad. The exposed pad (EP) on the package bottom must be attached to a heat-sinking conduit. The exposed pad may only be electrically connected to $V_{\mbox{\scriptsize EE}}.$

1. In the differential configuration when the input termination pins (VTD/VTD) are connected to a common termination voltage or left open, and if no signal is applied on D/D inputs, then the device will be susceptible to self oscillation.

### Table 2. ATTRIBUTES

Characteris	Value			
ESD Protection	> 2 kV > 200 V > 1 kV			
Moisture Sensitivity, Indefinite Time	Pb Pkg	Pb-Free Pkg		
	QFN-16	-	1	
Flammability Rating	UL 94 V-0 @ 0.125 in			
Transistor Count	225 D	evices		
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test				

2. For additional information, see Application Note AND8003/D.

### Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		3.8	V
V <sub>IN</sub>	Positive Input	GND = 0 V	$V_{IN} \leq V_{CC}$	3.8	V
I <sub>IN</sub>	Input Current Through $R_T$ (50 $\Omega$ Resistor)	Static Surge		35 70	mA mA
I <sub>OSC</sub>	Output Short Circuit Current Line-to-Line (Q to $\overline{Q}$ ) Line-to-End (Q or $\overline{Q}$ to GND)	$Q \text{ or } \overline{Q}$ $Q \text{ to } \overline{Q} \text{ to } GND$	Continuous Continuous	12 24	mA
T <sub>A</sub>	Operating Temperature Range	QFN-16		-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	QFN-16 QFN-16	41.6 35.2	°C/W °C/W
$\theta_{\text{JC}}$	Thermal Resistance (Junction-to-Case)	1S2P (Note 3)	QFN-16	4.0	°C/W
T <sub>sol</sub>	Wave Solder Pb Pb-Free			265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board - 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

Symbol	Characteristic	Min	Тур	Max	Unit
Icc	Power Supply Current (Note 8)		35	50	mA
DIFFERENTIAL INPUTS DRIVEN SINGLE-ENDED (Figures 15, 16, 20, and 22)					
V <sub>th</sub>	Input Threshold Reference Voltage Range (Note 7)	GND +100		V <sub>CC</sub> – 100	mV
V <sub>IH</sub>	Single-ended Input HIGH Voltage	V <sub>th</sub> + 100		V <sub>CC</sub>	mV
V <sub>IL</sub>	Single-ended Input LOW Voltage	GND		V <sub>th</sub> – 100	mV
DIFFERE	NTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 11, 12, 13, 14, 21, and 23)				
V <sub>IHD</sub>	Differential Input HIGH Voltage	100		V <sub>CC</sub>	mV
V <sub>ILD</sub>	Differential Input LOW Voltage	GND		V <sub>CC</sub> – 100	mV
V <sub>CMR</sub>	Input Common Mode Range (Differential Configuration)	GND + 50		V <sub>CC</sub> - 50	mV
V <sub>ID</sub>	Differential Input Voltage (V <sub>IHD</sub> - V <sub>ILD</sub> )	100		V <sub>CC</sub>	mV
R <sub>TIN</sub>	Internal Input Termination Resistor	40	50	60	Ω

LVDS OUTPUTS (Note 4)

V <sub>OD</sub>	Differential Output Voltage	250		450	mV
$\Delta V_{OD}$	Change in Magnitude of $V_{OD}$ for Complementary Output States (Note 9)	0	1	25	mV
V <sub>OS</sub>	Offset Voltage (Figure 19)	1125		1375	mV
$\Delta V_{OS}$	Change in Magnitude of $V_{OS}$ for Complementary Output States (Note 9)	0	1	25	mV
V <sub>OH</sub>	Output HIGH Voltage (Note 5)		1425	1600	mV
V <sub>OL</sub>	Output LOW Voltage (Note 6)	900	1075		mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. LVDS outputs require 100  $\Omega$  receiver termination resistor between differential pair. See Figure 18.

5.  $V_{OL}max = V_{OS}max + \frac{1}{2}V_{OD}max$ . 6.  $V_{OL}max = V_{OS}min - \frac{1}{2}V_{OD}max$ . 7.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.

8. Input termination pins open, D/D at the DC level within  $V_{CMR}$  and output pins loaded with  $R_L = 100 \Omega$  across differential. 9. Parameter guaranteed by design verification not tested in production.

			<b>−40°C</b>		25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
V <sub>OUTPP</sub>	$\begin{array}{l} \mbox{Output Voltage Amplitude (@ V_{INPPmin})} & f_{in} \leq 1.0 \mbox{ GHz} \\ \mbox{(Figure 4)} & f_{in} = 1.5 \mbox{ GHz} \\ & f_{in} = 2.0 \mbox{ GHz} \end{array}$	200	350 300 270		250 200 170	350 300 270		250 200 170	350 300 270		mV
f <sub>DATA</sub>	Maximum Operating Data Rate	1.5	2.5		1.5	2.5		1.5	2.5		Gb/s
t <sub>PLH</sub> , t <sub>PHL</sub>	Differential Input to Differential Output Propagation Delay	270	370	470	270	370	470	270	370	470	ps
t <sub>SKEW</sub>	Duty Cycle Skew (Note 11) Within Device Skew (Note 16) Device-to-Device Skew (Note 15)		8 5 30	45 25 100		8 5 30	45 25 100		8 5 30	45 25 100	ps
<sup>t</sup> JITTER	$\begin{array}{ll} \text{RMS Random Clock Jitter (Note 13)} & f_{in} = 1.0 \ \text{GHz} \\ f_{in} = 1.5 \ \text{GHz} \\ \text{Deterministic Jitter (Note 14)} & f_{DATA} = 622 \ \text{Mb/s} \\ f_{DATA} = 1.5 \ \text{Gb/s} \\ f_{DATA} = 2.488 \ \text{Gb/s} \end{array}$		0.5 0.5 6 7 10	1 1 20 20		0.5 0.5 6 7 10	1 1 20 20		0.5 0.5 6 7 10	1 1 20 20	ps
V <sub>INPP</sub>	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 12)	100		V <sub>CC</sub> - GND	100		V <sub>CC</sub> - GND	100		V <sub>CC</sub> - GND	mV
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times @ 250 MHz Q, G (20% – 80%)	70	120	170	70	120	170	70	120	170	ps

# Table 5. AC CHARACTERISTICS $V_{CC}$ = 3.0 V to 3.6 V, GND = 0 V; (Note 10)

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Measured by forcing V<sub>INPPmin</sub> with 50% duty cycle clock source and V<sub>CC</sub> – 1400 mV offset. All loading with an external  $R_L = 100 \Omega$  across "D" and "D" of the receiver. Input edge rates 150 ps (20%–80%).

11. See Figure 17 differential measurement of tskew = |tPLH - tPHL| for a nominal 50% differential clock input waveform @ 250 MHz.

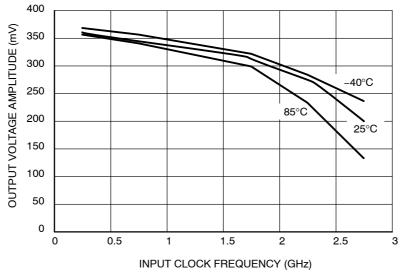
12. Input voltage swing is a single-ended measurement operating in differential mode.

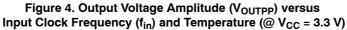
13. RMS jitter with 50% Duty Cycle clock signal at 750 MHz.

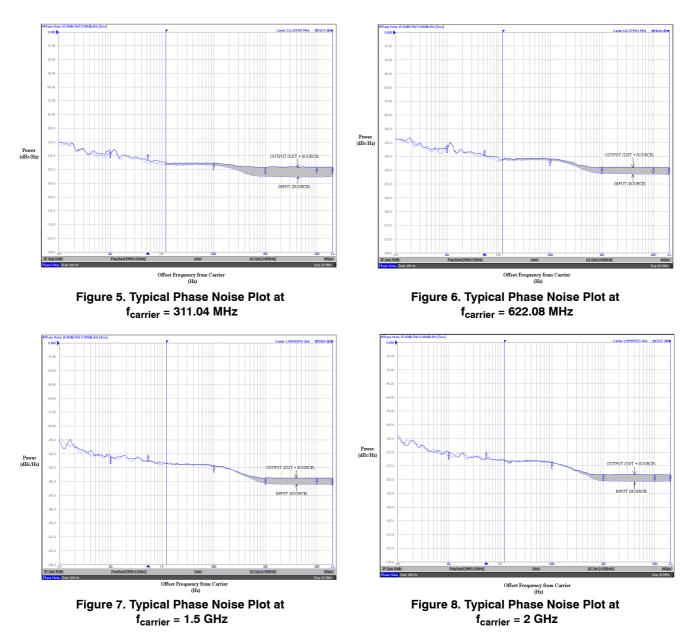
14. Deterministic jitter with input NRZ data at PRBS 223-1 and K28.5.

15. Skew is measured between outputs under identical transition @ 250 MHz.

16. The worst case condition between  $Q0/\overline{Q0}$  and  $Q1/\overline{Q1}$  from either  $D0/\overline{D0}$  or  $D1/\overline{D1}$ , when both outputs have the same transition.







The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6N11S device at frequencies 311.04 MHz, 622.08 MHz, 1.5 GHz and 2 GHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the

device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 96 fs, 40 fs, 15 fs and 14 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.



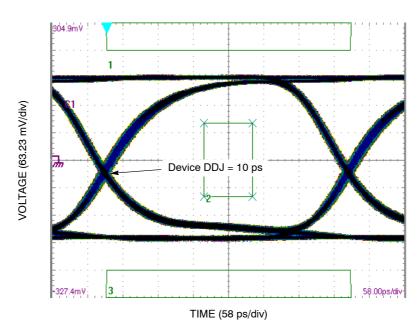


Figure 9. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23-1}$  and OC48 mask (V<sub>INPP</sub> = 100 mV; Input Signal DDJ = 14 ps)

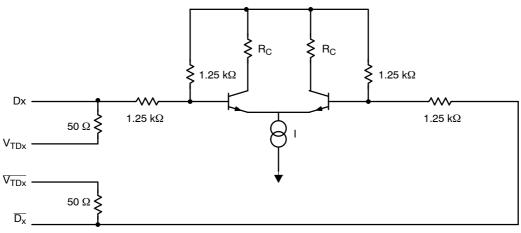


Figure 10. Input Structure

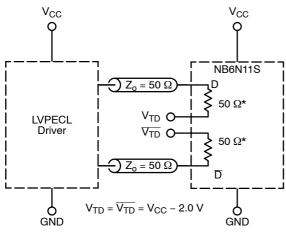


Figure 11. LVPECL Interface

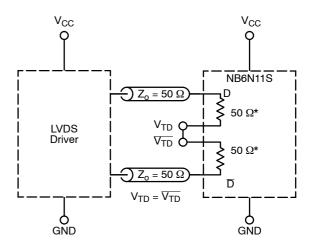


Figure 12. LVDS Interface

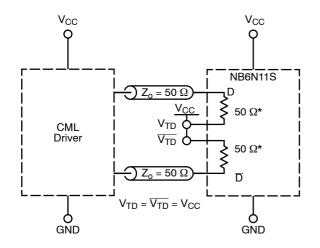


Figure 13. Standard 50  $\Omega$  Load CML Interface

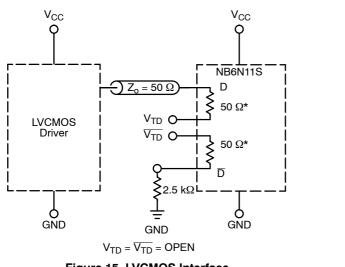


Figure 15. LVCMOS Interface

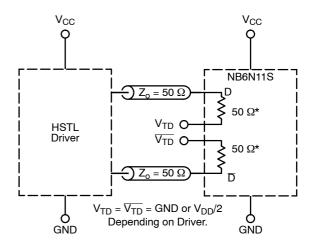


Figure 14. HSTL Interface

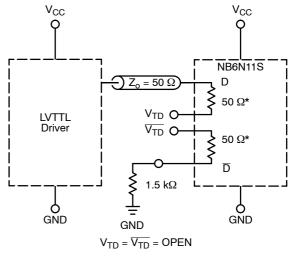


Figure 16. LVTTL Interface

\*R\_TIN, Internal Input Termination Resistor.

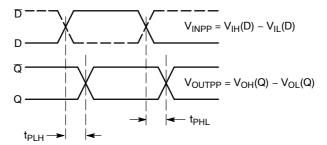


Figure 17. AC Reference Measurement

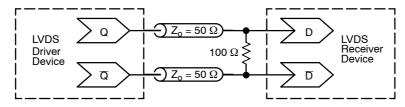
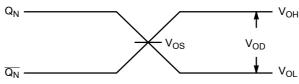


Figure 18. Typical LVDS Termination for Output Driver and Device Evaluation





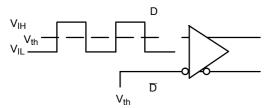
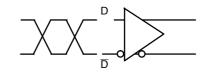
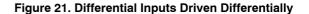


Figure 20. Differential Input Driven Single-Ended



 $V_{\text{CC}}$ 



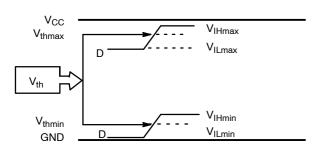
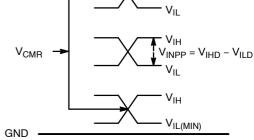


Figure 22. V<sub>th</sub> Diagram



VIH(MAX)

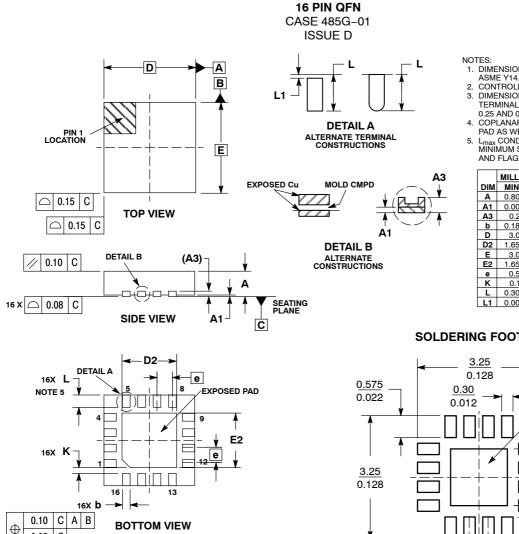
Figure 23. V<sub>CMR</sub> Diagram

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NB6N11SMNG	QFN-16, 3 X 3 mm (Pb-Free)	123 Units / Rail
NB6N11SMNR2G	QFN–16, 3 X 3 mm (Pb–Free)	3000 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

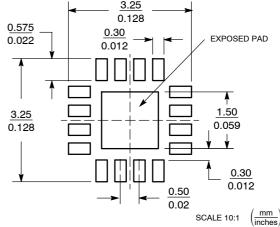


- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS. DIMENSION b APPLIES TO PLATED
- TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL. COPLANARITY APPLIES TO THE EXPOSED

PAD AS WELL AS THE TERMINALS. Lmax CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP

	MILLIMETER						
DIM	MIN	MAX					
Α	0.80	1.00					
A1	0.00	0.05					
A3	0.20	REF					
b	0.18	0.30					
D	3.00 BSC						
D2	1.65	1.85					
E	3.00	BSC					
E2	1.65	1.85					
е	0.50	0.50 BSC					
ĸ	0.18	TYP					
L	0.30	0.50					
L1	0.00	0.15					

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The products described herein (NB6N11S), may be covered by U.S. patents including 6,362,644. There may be other patents pending. AnyLevel and ECLinPS MAX are trademarks of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and 💷 are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All or operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

0.05 С NOTE 3

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative